IN THE SPECIFICATION

At page 6, after the last line, add:

--FIG. 17 shows a side view of a three dimensional electronic device packaging structure according to the present invention.

FIG. 18 shows a partial perspective view of the structure of FIG. 17.

FIG. 19 shows a top view of the electrical interconnection means of the structure of FIG. 17.

FIG. 20 shows a perspective view of the structures of FIG. 17 including a heat dissipation means.

FIG. 21 shows a cross sectional view of a section of the electrical interconnection means of the structure of FIG. 17.

FIG. 22 shows the structure of FIG. 21 disposed under pressure between two adjacent substrates.

FIG. 23 shows another embodiment of the structure of FIG. 21 having grooves on the two opposing surfaces.

FIG. 24 shows grooves on an interposer engaging projections on a substrate to align substrate and interposer contact locations.

FIG. 25 shows an alignment frame for mating with alignment grooves such as shown in the structure of FIG. 26.

FIG. 26 shows an interconnection structure having grooves for mating with the frame of FIG. 25.

FIGS. 27-35 show the process for making the electrical interconnection means, for example, of FIG. 21.

FIGS. 36 and 37 show an alternate embodiment of some of the method steps for fabricating an electrical interconnection means.

FIG. 38 is an enlarged view of the region of FIG. 23 enclosed in dashed circle 2230.

FIG. 39 schematically shows an optical system to form balls on the end of the wire conductors in FIG. 31.–

At page 8, amend the second paragraph as follows:

– In the embodiment of Figure 3, the pin 64 and socket 66 combination of the embodiment of Figure 2 is replaced by an interposer, such as, elastomeric connector 76. The structure of elastomeric connector 76 and the process for fabricating elastomeric connector 76 is described in copending US patent application Serial No. [07/963,364] 07/963,386 to B. Beaman et al., filed October 19, 1992, entitled "THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION MEANS" now issued as US 5,371,654, which is assigned to the assignee of the present invention, the teaching of which is incorporated herein by reference and of which the present application is a continuation-in-part thereof, the priority date of the filing thereof being claimed herein. The elastomeric connector can be opted to have one end permanently bonded to the substrate, thus forming a FRU (filed replacement unit) together with the probe/substrate/connector assembly. --

At page 6, amend lines 9-15, as follows:

-- Figures [7-13] 7-12 show the process for making the structure of Figure 5.

Figure [14] 13 shows a probe tip structure without a fan-out substrate.

Figure [15] 14 shows the elongated conductors of the probe tip fixed by solder protuberances to contact locations on a space transformation substrate.

Figure [16] 15 shows the elongated conductors of the probe tip fixed by laser weld protuberances to contact locations on a space transformation substrate.

Figure [17] 16 shows both interposer 76 and probe tip 40 rigidly bonded to space transformer 60.--

At page 17, before the last paragraph, add the following:

--US 5,371,654, entitled "THREE DIMENSIONAL HIGH PERFORMANCE INTERCONNECTION PACKAGE", incorporated by reference above, copied in its entirety here, is directed to a structure for packaging electronic devices, such as semiconductor chips, in a three dimensional structure which permits electrical signals to propagate both horizontally and vertically. The structure is formed from a plurality of assemblies. Each assembly is formed from a substrate having disposed on at least one surface a plurality of electronic devices. Each assembly is disposed in a stack of adjacent assemblies. Between adjacent assemblies there is an electrical interconnection electrically interconnecting each assembly. The electrical interconnection formed from an elastomeric interposer having a plurality of apertures extending therethrough. The array of apertures corresponds to the array of electronic devices on the substrates. The aperture and electrical interconnection is disposed over the array of electronic devices so that the electrical interconnection between adjacent electronic devices. The stack of assemblies is compressed thereby compressing the

electrical interconnection between adjacent assemblies. Methods for fabricating the electrical interconnection as a stand alone elastomeric sheet are described.

The US 5,371,654 invention is directed to packaging structures for interconnecting electronic devices in a three dimensional structure. More particularly, the present invention is directed to a structure having a plurality of substrates wherein each substrate has a plurality of electronic devices thereon forming an assembly. There are a plurality of assemblies disposed one on top of each other with a vertical wiring interconnection structure disposed between adjacent assemblies. Most particularly, the vertical wire interconnection structure contains a plurality of electrical conductors disposed in an elasometeric material and is compressed between adjacent assemblies.

In the microelectronics industry, integrated circuits, such as semiconductor chips, are mounted onto packaging substrates to form modules. In high performance computer applications, these modules contain a plurality of integrated circuits. A plurality of modules are mounted onto a second level of packages such as a printed circuit board or card. The cards are inserted in a frame to form a computer.

In nearly all conventional interconnection packages except for double sided cards, signals from one chip on the package travel in a two dimensional wiring net to the edge of the package then travel across a card or a board or even travel along cables before they reach the next package containing the destination intergrated circuit chip. Therefore, signals must travel off of one module onto wiring on a board or onto wiring on a cable to a second module and from the second module to the destination integrated circuit chip in the module. This results in long package time delays and increases the wireability requirement of the two dimensional wiring arrays.

An improvement in interchip propagation time and increase in real chip packaging density can be achieved if three dimensional wiring between closely spaced planes of chips could be achieved.

U.S. patent application Ser. No. 5,099,309 describes a three dimensional semiconductor chip packaging structure which comprises a plurality of stacked cards. Each card is specially fabricated to have cavities on both sides thereof which contain chips. On each surface of the card, there are electrical conductors which are bonded by wires to contact locations on the chips. Electrical conductors extend through the cards between the chip containing regions and to contact locations on each side of the card. These contact locations have dendrites on the surface. The cards are stacked so that the dendrite covered contact locations on adjacent sides of adjacent cards intermesh to provide electrical interconnection between the adjacent cards. This structure requires a high degree board flatness for the connections to be mated.

It is an object of the incorporated US 5,371,654 invention to provide improved three dimensional integrated circuit packaging structures.

Another object of the incorporated US 5,371,654 is to provide such a packaging structures with both horizontal electrical interconnections and compliant vertical electrical interconnections.

A further object of the incorporated US 5,371,654 is to provide such structures which can be assembled and disassembled into a plurality of subassemblies.

An additional object of the incorporated US 5,371,654 is to provide such structures which have a high thermal dissipation capacity.

Yet another object of the incorporated US 5,371,654 is to provide such structures which does not require rigid electrical interconnection between subassemblies.

Yet a further object of the incorporated US 5,371,654 invention is to provide such structures which can be fabricated using conventional packaging substrates.

A broad aspect of the incorporated US 5,371,654 invention is a structure having a plurality of assemblies. Each of the assemblies is formed from a substrate having a first and second opposing surfaces. There are a plurality of electronic devices disposed on at least one of the first and second surface of the substrate of each assembly. Each of the plurality of assemblies is disposed adjacent another of the plurality of assemblies so that the first surface of one of the adjacent assemblies is adjacent the second surface of the other of the adjacent assemblies. An electrical interconnection means is disposed between the first and second surfaces of the adjacent assemblies and provides electrical interconnection between contact locations on the adjacent surfaces. The electrical interconnection means is formed from a dielectric material having first and second opposing surfaces and a plurality of electrical contact locations on each surface which are electrically interconnected by a plurality of electrical conductors extending from the first surface to the second surface of the electrical interconnection means.

In a more particular aspect of the incorporated US 5,371,654, the substrates of the assemblies are formed from a diamond like material which has high thermal dissipation capacity.

In another more particular aspect of the incorporated US 5,371,654, the substrates have a plurality of dielectric and electrically conducting layers.

In another more particular aspect of the incorporated US 5,371,654, a heat dissipation means dissipates heat generated in the structure.

FIG. 17 shows structure 322 according to the present invention having two subcomponent assemblies 340 and 360. Structure 320 can have any number of subcomponent assemblies. Each subcomponent assembly is formed from a substrate 380 having a surface 210 which has a multilevel wiring structure 212 formed thereon. Multilevel wiring structure 212 is formed from a dielectric material, such as an oxide, a glass, a polymer and a ceramic, most preferably a polyimide polymer. Multilevel wiring

structure 212 contains at least one layer of electrical conductors 214, such as copper, aluminum and gold, and has on surface 216 a plurality of contact locations 218. Substrate 380 is shown in FIG. 17 as having vias 220 extending from surface 210 to surface 222. Surface 222 has a multilayer wiring structure 224 which is similar to multilayer wiring structure 212. Surface 226 of multilayer wiring structure 224 contains at least one electrically conductive layer 228 which is preferably copper, the dielectric material being preferably polyimide. Surface 226 has a plurality of electrical contact locations 230 which are preferably copper coated with gold. Electrical contact layers 218 are also preferably copper with a top coating of gold.

Substrate 380 can be any commonly used multilayered packaging substrate containing a plurality of electrical conductors or glass ceramic and is preferably a highly thermally conductive material such as synthetic diamond, aluminum nitride ceramic, silicon, a metal (such as copper) with an electrically insulating coating. Substrate 380 preferably has electrically conductive studs or vias 220 or through holes with a sidewall plated with an electrical conductor, such as copper, palladium, platinum and gold, as is commonly known in the art.

The electrical conductors in multilayer structures 212 on surface 210 of substrate 380 are electrically interconnected to contact locations 232 which are connected to via or stud 220 in substrate 380. Electrical conductors 228 in multilayer structure 224 on surface 222 of substrate 380 are electrically interconnected to contact locations 234 which are electrically interconnected to vias or studs 220 in substrate 380. Contact locations 232 and 234 are preferably formed from copper having a top surface of gold.

A plurality of electronic devices 236 and 238, such as integrated circuit chips, preferably semiconductor chips, are mounted onto surface 216 of multilayer wiring structure 212.

Electronic device 236 is mounted in a flip-chip-configuration onto surface 216 with solder mounds 240, commonly known as C4s, electrically interconnecting the electronic device 236 to the contact locations 218.

Electronic device 238 is mounted with active face 242 facing upwards and its nonactive face 244 in contact with surface 216 of multilayer structure 212. Alternatively, for better thermal contact to substrate 380, device 238 may be mounted directly with its nonactive face 244 in contact with surface 210 of substrate 380. This is accomplished by removing a section of multilayer structure 212. Wires 246 commonly made of aluminum or gold are bonded between contact location 218 and contact location 247 on surface 242 of electronic device 238. Wires 246 are bonded by commonly known wire bonding techniques, ultrasonic bonding techniques, laser bonding techniques and the like.

Disposed between electronic devices 236 and 238 there is an electrical interconnection means 249 details of which will be described hereinbelow.

The electrical interconnection means 249 has a top surface 248 having contact locations 250 and a bottom surface 252 having contact locations 254. Contact locations 254 are in electrical interconnection with contact locations 218 between chips 236 and 238. Contact locations 250 are in electrical interconnection with contact locations 230 on surface 226 of multilayer structure 224.

FIG. 18 shows a partial view of the structure of FIG. 17 in perspective with a region of the right forward most corner of each substrate 380 partially cut away to reveal vias or studs 220. On surface 216, there is seen contact locations 218 and electrical conductors 260 which electrically interconnect some of the contact locations 218. The electrical interconnection means 249 is shown only partially as a plurality of electrical conductors 262 and 264. The electrical interconnection means will be described in greater detail hereinbelow.

FIG. 19 shows a top view of one of the subcomponent assemblies 340 or 360 of FIG. 17 showing the electrical interconnection means 249 having a plurality of apertures 266. The apertures 266 are adapted to receive a plurality of electronic devices 268 which are

disposed on surface 216 of multilevel wiring structure 212 of FIG. 17. Numbers common between FIGS. 17, 18 and 19 represent the same thing.

FIG. 20 shows a perspective view of the structure shown in FIG. 17 plus heat dissipation means 251 and 253. Numbers common between FIGS. 17, 18, 19 and 20 represent the same thing. Heat dissipation means 251 and 253 are in thermal contact with substrates 380. The heat dissipation means is preferably made of aluminum. Substrate 380 is held in grooves in heat dissipation means 251 and 253 to ensure good thermal contact, mechanical support and compresses the interconnection means 249 between adjacent assemblies to provide electrical interconnection therebetween as described herein below. Heat dissipation means 251 and 253 are held in a support frame (not shown).

The thin film wiring layers 212 and 214 of FIG. 17 preferably contain at least one plain pair (XY) of wiring and two reference planes which provide power and ground to the electronic devices 236 and 238. If the electronic devices are bipolar chips there are preferably two additional power planes. The dimensions of the wiring and the thickness of the reference planes depends on the specific application and it can vary from 380 micron wide lines, 5 micron thick, on a 25 micron pitch to 25 micron wide lines, 25 microns thick on a pitch of 75 micron or more. The thickness of the insulation in the thin film wiring layers 212 and 224 is adjusted to provide the required transmission line impedance that is typically in the range of 4 to 80 ohms.

The electrical interconnection means 249 is formed to occupy the space between the chips as shown in FIGS. 17-20. The structure of FIG. 17 is compressed from the top and bottom of the structure to compress the electrical interconnection means 246 between the adjacent assemblies pressing electrical contact locations 230 on substrate 380 in contact with electrical contact locations 250 on electrical interconnection means 249 and pressing electrical contact locations 254 on electrical interconnection means 249 in contact with electrical contact locations 218 on the surface of the thin film wiring layer 212. Thus, a signal from any one chip will travel in the thin film wiring layer and

vertically through the electrical interconnection wiring means 249 to any thin film wiring plane in the stack of substrates 380 and thus along the shortest path to any chip in the entire structure 2. If a single plane contained 25 chips, for example, as shown in FIG. 19, each being 1 centimeter square, then the electrical interconnection means 246 would occupy the 1 centimeter space between each chip. With this design point the vias in the substrates 380 and the connections in the electrical interconnection means 249 could be made on a 36 mil square grid with 20 mil wide pads 218 on the substrate 380. There would be approximately 6,694 vertical signal connections possible on one plane. The grid could be reduced by a factor of approximately 2 if required and 26,000 vertical connections could be made.

The overall high performance package can consist of as many insulating plates populated by chips as required. The heat would be conducted to the edges of the high thermal conductivity substrates 380 where it would be carried away by air or water cooled or the like heat sinks as appropriate and commonly known in the art.

The substrates are preferably made of a high thermally conductive insulating material made of commercial diamond (manufactured for example by NORTON Inc. and Diamonex Inc.) which can be laser drilled to form vias and metallized for through hole connections using standard processing such as the process used on diamond heat spreaders for diode lasers. The very high thermal conductivity of diamond (1500 W/m° K.) makes it the most desirable material in this structure and would allow the cooling of more than 100 watts per plane. Other materials are useful. A lower cost alternative would be AnN ceramic with co-sintered solid vias, which are commercially available or silicon wafers which can contain laser drilled holes or chemically etched through vias. The thin film wiring layer 212 and 224 preferably contains copper wiring in a polyimide dielectric and can be fabricated by standard sequential thin film processes directly onto substrate 380 as described in R. Tummala and E. Rymasizewski, Microelectric Packaging Handbook, Van Nostrand, Rienhold, N.Y., 1989 Chapter 9, the teaching of which is incorporated herein by reference. The thin film wiring structure can be fabricated separately by the serial/parallel thin film wiring process and joined to the

substrates 380 as described in U.S. patent application Ser. No. 07/695,368, filed May 3, 1991, the teaching of which is incorporated herein by reference. In the serial/parallel processes the thin film wiring structures are fabricated on separate carriers then transferred and laminated to the insulated plates preferably by thermal compression bonding. The electrical interconnection means 249 preferably contains gold wires held at a slight angle in an elastomeric matrix. Other embodiments of large area array connectors can also work. The electrical interconnection means 249 using an elastomeric matrix has desirable properties such as lower resistance, low contact force, wipe, and low inductance which makes it particularly desirable in this application. The electrical interconnection means 249 can be fabricated to be approximately 1 millimeter thick with 10 percent compliance.

The substrates 380 are made with conducting vias. Top and bottom surface pads are applied by standard techniques such as evaporation of metals through a metal mask as described in Tiemmala et al., chapter 9 above. The electronic devices 36 and 38 are joined to each thin film wiring layer after the electronic devices are tested and burned in. The electrical interconnection means 249 are fabricated separately and tested. Finally, the stack of assemblies with electronic devices mounted onto the substrates with the electrical interconnection means 249 disposed thereon are aligned and a compressive force is applied to make the interconnections. The force is preferably from 10 to 50 grams per contact or from 70 to 300 kilograms for the entire package. The connection is separable.

FIGS. 21-37 show the method for fabricating electrical interconnection means 249 of FIG. 33 and show various embodiments and fabrication techniques of this electrical interconnection means.

FIG. 21 shows electrical interconnection means 280 which corresponds to electrical interconnection means 249 of FIG. 33. The electrical interconnection means 280 is formed from an elastomeric material 282 having a plurality of electrical conductors 284 extending from side 286 to side 288 thereof. Each conductor 284 preferably has a

generally spherical end 290 at side 286 and a flattened spherical shape 292 at side 288. The conductors 284 are preferably gold, gold alloy or copper alloy. The size, shape and the spacing of wires 284 along with the material properties of the elastomeric material 282 can be modified to optimize the connector for a specific application.

FIG. 22 shows substrate 294 and 296 pressed towards each other as indicated by arrows 298 and 2100 with interposer 280 therebetween. The elastomer 282 acts as a spring to push the enlarged end contact surfaces 290 and 292 against mating contacts 2104 and 2106 on substrates 294 and 296 respectively. Surface 2102 of substrate 294 has contact locations 2104 which are typically metallized pad. Substrate 296 has contact locations 2106 which are also typically metallized pads. When substrate 294 is pressed towards substrate 296 the ends 290 and 292 move laterally with respect to the contact surface because conductors 284 are at a nonorthogonal angle with respect thereto. This lateral movement results in a wiping action which breaks a surface oxide which is on the surface of the contact locations 2104 and 2106 and which is on the surface of the enlarged ends 290 and 292. The wiping action makes a good electrical contact between the enlarged surface 290 and 292 and the contact locations 2104 and 2106, respectively.

The advantages and unique features of the electrical interconnection means 280 are that it provides uniform spacing of the electrical conductors 284 and the elastomer material on, for example, a 0.008 inch minimum pitch using a single wire per contact. The enlarged ball shaped contacts 290 protrude from top side 286 of interconnection means 280 and the enlarged, flattened contacts 292 are generally flush with the bottom surface 288 of interconnection means 280. Textured or raised contact surface can be formed on the bottom side of the contact 292 to enhance the contact interface to an electrical contact location on substrate 296. The wires 284 in the elastomer material 282 can be grouped into small clusters to provide redundant connections for each contact location 2104 or 2106. If clustered wires are used, wires 295 in interconnect structure 280 of FIG. 22 would be eliminated.

FIG. 23 shows a cross section of another embodiment 2110 corresponding to the electrical interconnection means 249 of FIG. 17. Structure 2110 has electrical conductors 2112 which are clustered into groups 2114. Between each group there are grooves 2116. The elastomer material 2118 is preferably a silicone elastomer and there are ball shaped contacts 2120 on side 2122 and flat contact 2124 on side 2126 having a raised surface 2128. The top and bottom wire shapes can be varied for optimization. The alignment grooves 2116 of structure 2110 can be formed using a laser, electron beam or other sensing techniques as described in U.S. Pat. No. 4,998,885, to Beaman, the teaching of which is incorporated herein by reference.

Alignment features 2116 can be molded into the elastomer material to allow accurate alignment of the conductors 2112 in the structure 2110 with contact locations 2104 and 2106 on surfaces 2102 and 2105, respectively, as shown in FIG. 22. An alignment mechanism is preferred to enhance accurate positioning of the interposer wires with the contacts on the adjacent substrates. The molded alignment features can also be used to control the shrinkage and distortion of the contact grid in the elastomer material. Mechanically or thermally induced stress in the elastomer material can cause the interposer or distort causing alignment problems with the mating contacts.

The electrical interconnection means shown in FIGS. 21, 23 and 24 and electrical interconnection means 249 of FIG. 17 will also be referred to herein as an ELASTICON interposer. The ELASTICON interposer is designed to provide signal and power connections from the bottom surface of a substrate to another substrate. The ELASTICON interposer can be fabricated to have a full array of conductors or a clustered array of conductors. The interposer connector that uses a full array of conductors (or wires) would typically not require alignment of the connector to the contact locations on the substrate between which is disposed. By using clusters of wires, overall fewer wires are used to fabricate the interposer. This is useful for reducing the cost of the connector and the pressure required to ensure full engagement of the contacts. Interposer contacts that use a clustered array of wires preferably have

a means for aligning the wire clusters with the remaining said contacts. An interposer having a cluster set of wires minimizes the number of wires required during the interposer fabrication and enhances the compliance of the connector assembly. The molded or scribed grooves or other features in the elastomer material can be used to allow the interposer connector to self align with similar features on the substrates between which it is disposed as shown in FIG. 24. FIG. 24 shows interposer 2119 disposed on substrate 2121. Interposer 2119 has grooves 2123 which mate with projections 2125 on substrate 2121 which aligns substrate pads 2127 to interposer contact locations 2129. These alignment features can be designed using a variety of simple geometric shapes such as circular post, rectangular ridges, or a raised grid pattern. FIG. 26 shows a perspective view of an ELASTICON interposer useful as the electrical interconnection means 249 of FIG. 17. The ELASTICON interposer 2134 of FIG. 26 has a plurality of alignment grooves 2136 and regions 2138 containing clustered contacts wherein each region is surrounded by grooves 2140.

FIG. 25 shows an alignment frame 2142 which is adapted for engagement with the grooves on the interposer 2134 of FIG. 26 to align substrate contact locations to interposer contact locations. For example, bar 2144 in alignment frame 2142 engages groove 2146 of structure 2134 of FIG. 26 and bar 2148 of frame 2142 engages groove 2150 of structure 2134 of FIG. 26. The frame is disposed on a substrate having contact locations to which interposer contact locations are to be aligned.

An overall alignment scheme is preferred to fabricate the structure of FIG. 17. Each of the disconnectable elements of the module preferably have a means of alignment to the other elements in the module. A separate alignment frame could be attached to each substrate similar to the one used for the interposer.

FIGS. 27-35 show a fabrication method for the ELASTICON interposers described herein.

The fabrication process starts with a sacrificial substrate 2160, which is preferably copper, copper/Invar/copper or copper/molybdenium copper. Materials other than copper can be used such as aluminum, hard plastic or steel. The substrate 2160 can be fabricated to have protuberances 2162 which provide the grooves 2116 in the ELASTICON interposers of FIG. 23. The protuberances 2162 can be formed using various fabrication techniques including machining of the surface 2164 or stamping of the surface 2164. After the substrate has been formed with the protuberances, the top surface 2164 is sputtered or plated with soft gold or Ni/Au to provide a suitable surface for thermosonic ball bonding. Other bonding techniques can be used such as thermal compression bonding, ultrasonic bonding, laser bonding and the like. A commonly used automatic wire bonder is modified to ball bond gold, gold alloy, copper, copper alloy, aluminum, nickel or palladium wires 2166 to the substrate surface 2164 as shown in FIG. 27. The wire preferably has a diameter of 0.001 to 0.005 inches. If a metal other than Au is used, a thin passivation metal such as Au, Cr, Co, Ni or Pd can be coated over the wire by means of electroplating, or electroless plating, sputtering, e-beam evaporation or any other coating techniques known in the industry. Structure 2168 of FIG. 27 is the ball bonding head which has a wire 2170 being fed from a reservoir of wire as in a conventional wire bonding apparatus. FIG. 27 shows the ball bond head 2168 in contact at location 2169 with surface 2164 of substrate 2160.

FIG. 28 shows the ball bonding head 2168 withdrawn in the direction indicated by arrow 2171 from the surface 2164 and the wire 2170 drawn out to leave disposed on the surface 2164 wire 2166. In the preferred embodiment, the bond head 2168 is stationary and the substrate 2160 is advanced as indicated by arrow 2161. The bond wire is positioned at an angle preferably between 5° to 60° from vertical and then mechanically severed by knife edge 2172 as shown in FIG. 29. The knife edge 2172 is actuated, the wire 2170 is clamped and the bond head 2168 is raised. When the wire 2170 is severed there is left on the surface 2164 of substrate 2160 a flying lead 2166 which is bonded to surface 2164 at one end and the other end projects outwardly away from the surface. A ball can be formed on the end of the wire 2166 which is not bonded to surface 2164 using a laser or electrical discharge to melt the end of the wire.

Techniques for this are commonly known in the art. A split beam laser delivery systems, described hereinbelow, is used to localize the laser energy to a single wire for forming the ball. This minimizes the laser energy absorbed by adjacent wires that could cause the wires to deform. A ball is not required on the end of the wire. This modified wire bonding process is repeated to form a dense array of angled wires on the substrate.

FIG. 30 shows the wire 2170 severed to leave wire 2166 disposed on surface 2164 of substrate 2160. The wire bond head 2168 is retracted upwardly as indicated by arrow 2174. The wire bond head 2168 has a mechanism to grip and release wire 2170 so that wire 2170 can be tensioned against the shear blade to sever the wire.

FIG. 31 shows that the wire is severed, the bond head is raised to a "home" position. An electronic flame off unit (part of Hughes Wire Bonder, Modec III-2640) electrode is positioned below the bond head and an electrical discharge from the electrode is used to melt the wire in the capillary tip to form a ball.

After the wire bonding process is completed, the substrate 2160 is placed in a casting mold 2190 as shown in FIG. 32. A controlled volume of liquid elastomer 2192 is disposed into the casting mold and allowed to settle out (flow between the wires until the surface is level) before curing as shown in FIG. 33. Once the elastomer has cured, the substrate is extracted from the mold as shown in FIG. 34 and indicated by arrow 2194. The cured elastomer is represented by reference rule 2196. Opening 2161 in mold 2190 is a tooling feature for extracting the substrate from the mold. The structure 2198 is removed from the mold 2190 and is placed in a sulfuric and nitric acid bath 2200, as shown in FIG. 35 to dissolve the copper substrate 2160. Ultrasonic agitation of the sulfuric and nitric acid helps to facilitate the etching of the copper substrate and causes the gold plating on the surface of the copper substrate to flake off from the surface 2202 of the elastomer material 2196 leaving the surface of the ball bonds 2204 exposed.

Alternatively, the substrate can be made of peel-apart-copper, where a thin layer of copper is attached to a solid substrate with a marginal adhesion strength. After the fabrication is completed, the connector can be peeled off from the sacrificial substrate before the remaining thin copper is flash etched away.

A high compliance, high thermal stability siloxane elastomer material is preferable for this application. The high temperature siloxane material is cast or injected and cured similar to other elastomeric materials. To minimize the shrinkage, the elastomer is preferably cured at lower temperature ($T \leq 60°$) followed by complete cure at higher temperature ($T \geq 80°$). To further control the shrinkage, the connector is cast into a plastic frame, which was predrilled with holes around its periphery. When the elastomer is poured into this frame a physical locking of the elastomer to the frame takes place which both holds the elastomer/connector to the frame and minimizes the shrinkage. To improve the compliance and reduce the dielectric constant of the elastomer material, a foam agent can be blended into the commercial elastomeric material at a ratio ranging from 10 to 60%. Also, foam can be employed as a distinct layer.

Among the many commercially available elastomers, such as ECCOSIL and SYLGARD, the use of polydimethylsiloxane based rubbers best satisfy both the material and processing requirements. However, the thermal stability of such elastomers is limited at temperatures below 200° C. and significant outgassing is observed above 100° C. We have found that the thermal stability can be significantly enhanced by the incorporation of 25 wt % or more diphenylsiolxane (FIG. 17). Further, enhancement in the thermal stability has been demonstrated by increasing the molecular weight of the resins (oligomers) or minimizing the crosslink junction. The outgassing of the elastomers can be minimized at temperatures below 300° C. by first using a thermally transient catalyst in the resin synthesis and secondly subjecting the resin to a thin film distillation to remove low molecular weight side-products. For our experiments, we have found that 25 wt % diphenylsiloxane is optimal, balancing the desired thermal stability with the increased viscosity associated with diphenylsiloxane

incorporation. The optimum number average molecular weight of the resin for maximum thermal stability was found to be between 18,000 and 35,000 g/mol. Higher molecular weights were difficult to cure and too viscous, once filled, to process. Network formation was achieved by a standard hydrosilylation polymerization using a hindered platinum catalyst in a reactive silicon oil carrier.

In FIG. 27 when bond head 2168 bonds the wire 2170 to the surface 2164 of substrate 2160 there is formed a flattened spherical end shown as 2204 in FIG. 35. The protuberances 2162 on substrate 2160 as shown in FIG. 27 result in grooves in the elastomer such as grooves 2116 shown in FIG. 23. These grooves form alignment features. The design and tolerances used to form the copper substrate 2160 are preferably carefully matched with the design and tolerances used to fabricate the alignment features on the substrates 294 and 296 shown in FIG. 22. Alternatively, on a substantially flat substrate, an alignment frame, such as shown in FIG. 25, can be disposed on the surface of a substrate, such as 294 and 296, of FIG. 22 and the elasticon interposer with grooves can be disposed onto this alignment frame so that the alignment grooves of the interposer engage the frame pattern as described herein above with respect to FIGS. 25 and 26.

Referring to FIG. 36, multiple substrates 2210 each having a group of wires 2212 disposed thereon can be placed into a common mold 2214 into which the liquid elastomer 2216 as described herein above is disposed and cured. The cured elastomer links the substrates together into a single interposer 2218 as shown in FIG. 37. Grooves 2211 are for compliance or alignment requirements. Alternatively, several smaller connectors can be fabricated on the same substrate as a single unit and then separated after the elastomer is cured and the substrate is etched away.

Also, the surface of the copper sacrificial substrate can be textured or embossed prior to gold plating and wire bonding to provide a textured or raised contact surface on the bottom of the ball bonds. The completed interposer 2218 of FIG. 37 can be further modified by using a laser to scribe channels in the elastomeric material between the

bond wires at an angle matching the angle of the bond wires, as shown in FIG. 23. The criss-crossing channels create independent elastomeric columns (shown in FIG. 26 as 2138) surrounding the gold wires. This would allow individual wires or groups of wires to compress independently and allow the interposer to compensate for slight variations in the remaining surfaces while reducing the total pressure required to compress the entire interposer. Patterned connectors can easily be fabricated by programming the wire bonder to a specific pattern and molding the elastomer to provide holes or open areas in the connector that correspond with other electronic or mechanical components surrounding the connector.

To improve compliance and reduce wire deformation, grooves are preferably molded into the elastomer on both sides of the connector surfaces in both the X and Y directions or in a circular geometry. The width and depth of the groove are preferably wider than 5 mils and deeper than 10 mils, respectively, in an interposer 100 mils thick. The grooves are preferably molded in a direction parallel to the angled wire.

Grooves have been fabricated with laser, electron beam, metal mask and slicing with a blade. Other techniques such as stamping, injection molding and other known techniques to create the desired geometry would also work well.

The contact balls at the end of the wires are formed using a split beam laser configuration. The end of each wire will melt and form the ball only at the point where the two beams intersect. The design is illustrated in FIG. 36 which shows light source 2300, preferably an argon-ion laser which is the source of light beam 2302 which is reflected as light beam 2304 by mirror 2306. Light beam 2304 is directed through light beam expander 2308 to form expanded light beam 2310. Expanded light beam 2310 is directed to beam splitter 2312 which splits beam 2310 into beams 2314 and 2316. Beam 2316b is reflected off mirror 2322 as light beam 2324. Beam 2314 is reflected off mirror 2318 as light beam 2320. Beam 2320 is passed through focusing lens 2328 to form focused beams 2330 which focused onto spot 2332 on the workpiece which is the end of a wire. Beam 2324 is passed through focusing lens 2334 to form focused

beam 2336 which is focused onto spot 2332 on the workpiece. The workpiece is disposed on x–y table 2338. The beam is expanded before focusing to get the desired size of spot 2332.

FIG. 37 shows an enlarged view of the region of FIG. 23 enclosed in the dashed circle 2230. Element 2124 is a flattened ball shape member at the end of conductor 2112. The flattened ball shaped member 2124 was formed when conductor 2112 was wire bonded to the sacrificial copper layer as described with reference to FIG. 27. The sacrificial copper layer can be fabricated with an array of pits in the surface in the regions where the wires 2112 are bonded. These pits can have, for example, a hemispherical shape, rectangular shape, pyramidal shape or any other shape. If such an array of pits are used and the wire is bonded in the region of the pit, a protuberance such as 2128 of FIG. 36 is formed at the surface 2232 of flattened ball. This protuberance provides a projecting region to the contact formed by flattened ball 2124 which can wipe on the surface of the contact location to which the flattened ball is to be electrically connected.--